Notice of Allowability	Application No.	Applicant(s)	
	10/022,020	ZIEGLER ET AL.	
	Examiner	Art Unit	
	Inder P. Mehra	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment sated 12/19/05*.

2. ☒ The allowed claim(s) is/are *4,2,5-9,and 11-25(Renumbered as 1-22 respectively)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

DANG TON
PRIMARY EXAMINER

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This office action is in response to amendment dated: 12/19/2005.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Bryan W. Bockhop, Attorney, Regd. No. 39,613 on 2/23/06.

The application has been amended as follows:

3. Refer to claim 4. Replace claim 4 with the following claim 4:

4. (Currently Amended) A method of communicating a plurality of parallel data packets from a first ~~data~~ parallel data bus to a second parallel data bus, comprising the steps of:

   a. separating each of the plurality of parallel data packets into a first portion and a second portion;

   b. converting each of the first ~~portion~~ portions into a first serial data stream and converting each of the second ~~portion~~ portions into a second serial data stream;

   c. transmitting the first serial data stream over a first serial data channel and transmitting the second serial data stream over a second serial data channel;

   d. converting the first serial data stream into a plurality of first received portions and converting the second serial data stream into a plurality of second received portions; ~~and~~

e. combining selected first received portions with corresponding selected second received portions so as to regenerate the plurality of parallel data packets~~.~~;

f. receiving parallel data packets using a plurality of FIFO's, each FIFO having a read side and a write side

g. entering a first write state when either a write side error signal or a read asynchronous initialization request signal is asserted and performing the following operations:

   i. writing to all of the FIFO's is stopped; and

   ii. a write asynchronous initialization request signal is asserted;

h. exiting the first write state when an initialization signal is asserted,

i. entering a second write state from the first write state and de-asserting a write side initialization request signal;

j. exiting the second write state when the initialization signal is de-asserted;

k. entering a third write state from the second write state and resuming normal operations;

l. entering a first read state when either a read side error signal or ~~a~~ the write side initialization request signal is asserted, and performing the following operations:

   i. reading from all of the FIFO's is stopped; and

   ii. the read asynchronous initialization request signal is asserted;

m. exiting the first read state when all of the initialization request signals are asserted,

n. entering a second read state from the first read state and performing the following operations:

   i. asserting the initialization signal; and

   ii. de-asserting ~~the~~ a read initialization signal;

o. exiting the second read state when all of the initialization request signals are de-asserted; and

p. entering a third read state from the second read state and de-asserting the initialization signal.

Refer to claim 11. Replace claim 11 with the following claim11.

11. Currently Amended) An apparatus for transmitting a plurality of data words from a first parallel data bus to a second parallel data bus, comprising:

a. a first serializer, in data communication with a first parallel bus, that transforms a first portion of each data word into a first serial data stream;

b. a second serializer, in data communication with a second parallel bus, that transforms a second portion, different from the first portion, of each data word into a second serial data stream;

c. a first serial data channel, in data communication with the first serializer, upon which the first serial data stream is transmitted;

d. a second serial data channel, in data communication with the second serializer, upon which the second serial data stream may be transmitted;

e. a first de-serializer, in data communication with the first serial data channel, that transforms the first serial data stream into a plurality of first parallel data units, each first parallel data unit being identical to a corresponding first portion of a data word;

f. a second de-serializer, in data communication with the second serial data channel, that transforms the second serial data stream into a plurality of second parallel data units, each second parallel data unit being identical to a corresponding second portion of a data word; and

g. a receiver element that receives the first parallel data units from the first de-serializer and the second parallel data units from the second de-serializer and that assembles corresponding ones of the first parallel data units and the second parallel data units into corresponding data words and that transmits the corresponding data words to the second parallel data bus, the receiver element including:

i. a first A-FIFO that is capable of receiving packets of parallel data from the first de-serializer;

ii. a first B-FIFO that is capable of receiving packets of parallel data from the second de-serializer;

iii. a second A-FIFO that is capable of receiving packets of parallel data from the first A-FIFO;

iv. a second B-FIFO that is capable of receiving packets of parallel data from the first B-FIFO; and

v. a logic element that concatenates packets of parallel data from the second A-FIFO with packets of parallel data from the second B-FIFO to generate a data word and that transmits the data word to the second parallel data bus.

Refer to claim 17. Replace claim 17 with the following claim 17.

17. (Currently Amended) The apparatus of Claim 11, further comprising a error recovery logic element that embodies a state machine that includes the following elements:

a. a first write state, which is entered when either a write side error signal or a read asynchronous initialization request signal is asserted, which exited when an initialization signal is asserted, and in which the following operations are performed:

i. writing to all of the FIFO's is stopped; and

ii. a write asynchronous initialization request signal is asserted;

b. a second write state, which is entered from the first write state, which is exited when the initialization signal is de-asserted, and in which a write side initialization request signal is de-asserted;

c. a third write state, which entered from the second write state and in which normal operations are resumed;

d. a first read state which is entered when either read side error signal or a the write side initialization request signal is asserted, which is exited when all of the

initialization request signals are asserted, and in which the following operations are performed:

i. reading from all of the FIFO's is stopped; and

ii. the read asynchronous initialization request signal is asserted;

e. a second read state, which is entered from the first read state, which is exited when all of the initialization request signals are de-asserted, and in which the following operations are performed:

i. the initialization signal is asserted; and

ii. the read asynchronous initialization request signal is de-asserted; and

f. a third read state, which is entered from the second read state and in which the initialization signal is de-asserted.

Allowable Subject Matter

4. Claims 2, 4, 5-9 and 11-25 are allowed.

REASONS FOR ALLOWANCE

5. The following is an examiner's statement of reasons for allowance:

The prior art of record does not disclose or teach directly or indirectly the combination of the following limitations:

As recited by claim 4,

A method of communicating a plurality of parallel data packets from a first ~~data~~ parallel data bus to a second parallel data bus, comprising the steps of:

a. separating each of the plurality of parallel data packets into a first portion and a second portion;

b. converting each of the first ~~portion~~ portions into a first serial data stream and converting each of the second ~~portion~~ portions into a second serial data stream;

c. transmitting the first serial data stream over a first serial data channel and transmitting the second serial data stream over a second serial data channel;

d. converting the first serial data stream into a plurality of first received portions and converting the second serial data stream into a plurality of second received portions; ~~and~~

e. combining selected first received portions with corresponding selected second received portions so as to regenerate the plurality of parallel data packets~~.~~;

f. receiving parallel data packets using a plurality of FIFO's, each FIFO having a read side and a write side

g. entering a first write state when either a write side error signal or a read asynchronous initialization request signal is asserted and performing the following operations:

   i. writing to all of the FIFO's is stopped; and

   ii. a write asynchronous initialization request signal is asserted;

h. exiting the first write state when an initialization signal is asserted,

i. entering a second write state from the first write state and de-asserting a write side initialization request signal;

j. exiting the second write state when the initialization signal is de-asserted;

k. entering a third write state from the second write state and resuming normal operations;

l. entering a first read state when either a read side error signal or ~~a~~ the write side initialization request signal is asserted, and performing the following operations:

   i. reading from all of the FIFO's is stopped; and

   ii. the read asynchronous initialization request signal is asserted;

m. exiting the first read state when all of the initialization request signals are asserted,

n. entering a second read state from the first read state and performing the following operations:

   i. asserting the initialization signal; and

   ii. de-asserting ~~the~~ a read initialization signal;

o. exiting the second read state when all of the initialization request signals are de-asserted; and

p. entering a third read state from the second read state and de-asserting the initialization signal.

As recited by claim 11,

An apparatus for transmitting a plurality of data words from a first parallel data bus to a second parallel data bus, comprising:

a. a first serializer, in data communication with a first parallel bus, that transforms a first portion of each data word into a first serial data stream;

b. a second serializer, in data communication with a second parallel bus, that transforms a second portion, different from the first portion, of each data word into a second serial data stream;

c. a first serial data channel, in data communication with the first serializer, upon which the first serial data stream is transmitted;

d. a second serial data channel, in data communication with the second serializer, upon which the second serial data stream may be transmitted;

e. a first de-serializer, in data communication with the first serial data channel, that transforms the first serial data stream into a plurality of first parallel data units, each first parallel data unit being identical to a corresponding first portion of a data word;

f. a second de-serializer, in data communication with the second serial data channel, that transforms the second serial data stream into a plurality of second parallel data units, each second parallel data unit being identical to a corresponding second portion of a data word; and

g. a receiver element that receives the first parallel data units from the first de-serializer and the second parallel data units from the second de-serializer and that assembles corresponding ones of the first parallel data units and the second parallel data units into corresponding data words and that transmits the

corresponding data words to the second parallel data bus, the receiver element including:

i. a first A-FIFO that is capable of receiving packets of parallel data from the first de-serializer;

ii. a first B-FIFO that is capable of receiving packets of parallel data from the second de-serializer;

iii. a second A-FIFO that is capable of receiving packets of parallel data from the first A-FIFO;

iv. a second B-FIFO that is capable of receiving packets of parallel data from the first B-FIFO; and

v. a logic element that concatenates packets of parallel data from the second A-FIFO with packets of parallel data from the second B-FIFO to generate a data word and that transmits the data word to the second parallel data bus.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Inder P. Mehra whose telephone number is 571-272-3170. The examiner can normally be reached on Monday through Friday from 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Inder Pal Mehra 2/24/06

Inder P Mehra
Examiner
Art Unit 2666

DANG TON
PRIMARY EXAMINER